Please amend the claims as follows. This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-5 (cancelled)

Claim 6 (currently amended): A semiconductor device, comprising:

a substrate having transistor devices;

a plurality of copper interconnect metallization lines and conductive vias defined in each of a plurality of interconnect levels of the semiconductor device, the plurality of copper interconnect metallization lines and conductive vias being isolated from each other by a porous dielectric material; and

a plurality of supporting stubs, each of the plurality of supporting stubs configured to form a supporting column that extends through the plurality of interconnect levels of the semiconductor device, the plurality of supporting stubs not being electrically interconnected to the plurality of copper interconnect metallization lines and conductive vias.

Claim 7 (cancelled)

Claim 8 (currently amended): A semiconductor device as recited in claim 6, further comprising:

a passivation-capping layer defined over a topmost layer of the copper interconnect metallization lines and conductive vias.

Claims 9-25 (cancelled)

Claim 26 (previously added): A semiconductor device as recited in claim 6, wherein the plurality of copper interconnect metallization lines and conductive vias define dual damascene structures.

Claim 27 (previously amended): A semiconductor device as recited in claim 6, wherein the plurality of supporting stubs further support a passivation layer.

Claim 28 (currently amended): A semiconductor device, comprising:

a substrate having transistor devices; and

an intermetal dielectric layer including conductive contacts defining a first interconnect level of a plurality of interconnect levels of the semiconductor device;

a passivation layer defined over the ILD layer; and

a plurality of copper interconnect metallization lines and conductive vias defined in each ~~of a~~ remaining interconnect level of the plurality of interconnect levels of the semiconductor device defined over the passivation layer, the plurality of copper interconnect metallization lines and conductive vias being isolated from each other by a porous dielectric material.

Claim 29 (currently amended): A semiconductor device as recited in claim 28, further comprising:

a plurality of supporting stubs, each of the plurality of supporting stubs configured to form a supporting column that extends through each of the remaining interconnect level of the plurality of interconnect levels of the semiconductor device.

Claim 30 (previously added): A semiconductor device as recited in claim 29, wherein the plurality of supporting stubs is not electrically interconnected to the plurality of copper interconnect metallization lines and conductive vias.

Claim 31 (currently amended): A semiconductor device as recited in claim 28, further comprising:

a passivation-capping layer defined over a topmost layer of the copper interconnect metallization lines and conductive vias.

Claim 32 (previously added): A semiconductor device as recited in claim 28, wherein the plurality of copper interconnect metallization lines and conductive vias define dual damascene structures.

Claim 33 (currently amended): A semiconductor device as recited in claim 29, wherein the plurality of supporting stubs further support a passivation-capping layer.

Claim 34 (currently amended): A semiconductor device, comprising:

a substrate having transistor devices;

an intermetal dielectric layer (ILD) including conductive contacts defining a first interconnect level of a plurality of interconnect levels of the semiconductor device, the conductive contacts being isolated from each other by a non-porous dielectric;

a passivation layer defined over the ILD layer; and

a plurality of copper interconnect metallization lines and conductive vias defined in each of a remaining interconnect level of ~~a~~ the plurality of interconnect levels of the

semiconductor device, the plurality of copper interconnect metallization lines and conductive vias being isolated from each other by a porous dielectric material; and

a passivation-capping layer defined over a topmost layer of the copper interconnect metallization lines and conductive vias.

Claim 35 (currently amended): A semiconductor device as recited in claim 34, further comprising:

a plurality of supporting stubs, each of the plurality of supporting stubs configured to form a supporting column that extends through each remaining interconnect level of the plurality of interconnect levels of the semiconductor device.